L Number	Hits	Search Text	DB	Time stamp
1	1	("6261881").PN.	USPAT; US-PGPUB	2002/05/07 12:57
2	306	TFT and (irradiating with (infrared or laser or ultraviolet)) and wiring and insulating	USPAT; US-PGPUB	2002/05/07 13:22
3	145	(TFT and (irradiating with (infrared or laser or ultraviolet)) and wiring and insulating) and @ad<=19980821	USPAT; US-PGPUB	2002/05/07 12:58
4	134	((TFT and (irradiating with (infrared or laser or ultraviolet)) and wiring and insulating) and @ad<=19980821) and (amorphous with silicon)	USPAT; US-PGPUB	2002/05/07 13:00
5	105	(((TFT and (irradiating with (infrared or laser or ultraviolet)) and wiring and insulating) and @ad<=19980821) and (amorphous with silicon)) and (crystalliz$3 or crystallization)	USPAT; US-PGPUB	2002/05/07 13:01
6	71	((((TFT and (irradiating with (infrared or laser or ultraviolet)) and wiring and insulating) and @ad<=19980821) and (amorphous with silicon)) and (crystalliz$3 or crystallization)) and yamazaki	USPAT; US-PGPUB	2002/05/07 13:02
7	5	TFT and (irradiating with (infrared or laser or ultraviolet)) and wiring and insulating	EPO; JPO; DERWENT; IBM TDB	2002/05/07 13:22

DOCUMENT-IDENTIFIER: US 6323069 B1
TITLE: Method of manufacturing a thin film transistor using light irradiation
to form impurity regions

---------- KWIC ---------

BSPR:
As an active matrix circuit using TFT, two sorts of TFT, which employ such
polycrystal semiconductor as polycrystal **silicon and such amorphous**
semiconductor as **amorphous silicon,** have been known. The former has a
difficulty in preparation for a large picture owing to its preparing process,
and then the latter, which can be prepared at a temperature of 350 or below,
has been mainly used for a large picture.

BSPR:
FIG. 2 shows a preparing process of a conventional **amorphous silicon TFT** (an
inverse stagger type). As the substrate 201, such heat resistant and
non-alkali glass as Corning 7059 is used. Since the maximum temperature of
preparing process for the **amorphous silicon TFT** is around 350, it is required
that the material therefor be resistant up to this temperature. Especially in
case of a liquid crystal display panel, the material is in need of a heat
resistant property and a high glass transition temperature not to be distorted
by heat treatment. The Corning 7059 can meet for the need, as the glass
transition temperature thereof is a little lower than 600.

BSPR:
Next, a film is formed using materials such as aluminum or tantalum,a
patterning is effected using the mask 1 and the gate electrode 202 is formed.

In particular, in order to prevent a short circuit between the gate electrode
wiring and the upper **wiring** thereof, it is recommended to form the oxide film
203 on this gate electrode surface. An anode oxidation method is chiefly
employed in the forming way of the oxide film.

BSPR:
Next, an **amorphous silicon** film is formed, it is necessary to raise a
temperature of the substrate up to 250 to 300, in case a plasma CVD method is
used. The film thickness is desired as thin as possible, it is generally to be
10 to 100 nm, and preferably to be 10 to 30 nm. The **amorphous silicon** region
205 is formed by patterning with the mask 2 which later will become a channel
forming region of TFT. The situation so far is shown in FIG. 2(B).

BSPR:
Further, a silicon nitride film is formed all over the surface, which is
patterned with the mask 3 to get the etching stopper 206. This stopper is
prepared so that the **amorphous silicon** region 205 for a channel forming region
will not be etched by mistake in a later process, because the **amorphous silicon**
region 205 is as thin as 10 to 100 nm as aforementioned. Also, since the
amorphous silicon region under part of the etching stopper functions as a
channel forming region, the etching stopper is designed to overlap with the
gate electrode as fully as possible. A conventional mask alignment, however,
gives a somewhat discrepancy, then the patterning is carried out so as to
achieve an enough overlapping with the gate electrode.

BSPR:
After that, N-type or P-type conductivity silicon film is formed. An ordinary
amorphous silicon TFT is N-type one. This **silicon** film is

prepared to be a
microcrystal state, as an **amorphous silicon** is too low in a conductivity.
N-type microcrystal silicon film can be prepared at a temperature of 350 or
below by a plasma CVD method. But it is not low enough in resistance, and then
the thickness of 200 nm or more was required. P-type microcrystal **silicon** film
was too big in resistance to be used, it was, therefore, difficult to prepare a
P-channel type **TFT with an amorphous silicon**.

BSPR:
The silicon film prepared in this way is patterned using the mask 4 to form
N-type microcrystal silicon region 207. The situation so far is shown in FIG.
2(C), in which a function of TFT can not be realized, as (N-type) microcrystal
silicon film is connected with itself on the etching stopper. It is,
therefore, necessary to separate the connection, and the groove 208 is formed
by separating the connection using the mask 5. It is feared that even the
amorphous silicon region 205 as a base is etched out making a mistake, if there
is no etching stopper in this case. This is caused by the reason that the
microcrystal **silicon** region 207 is from several to some ten times or more as
thick as the **amorphous silicon** region thereunder.
Afterward, the **wiring** 209
and the pixel electrode 210 are prepared, using the masks 6 and 7 by a known
method, the situation of which is shown in FIG. 2(D).

BSPR:
In the method stated above, so many seven sheets of mask are used, and it is
worried that a yield will be lowered. Therefore, a decreasing way of the
number of masks has been proposed as will be described in the following;
Firstly, a gate electrode part is patterned on a substrate using the first

mask. Then, a gate insulating film is formed, further, an **amorphous silicon** film and a **silicon** nitride film (later will be an etching stopper) are continuously formed. Next, an etching stopper is formed by etching only the silicon nitride film in a way of self-alignment, using a gate electrode as a mask and exposing from the back. Then, thereon a microcrystal silicon film is formed, and a TFT region including a groove over the channel(corresponds to the numeral 208 in FIG. 2) is formed using the second mask. Afterward, a **wiring** and an electrode are formed using the third and fourth masks. Finally, the equivalent one as shown in FIG. 2(D) can be obtained. In such way, the number of masks can be reduced by three utilizing a self-alignment process.

BSPR:
However, any of these factors to cause the unevenness of TFT can not be cut down easily. Namely, the thinner a gate electrode part is, the higher the resistance of gate electrode **wiring** will be. On the other hand, in order to keep the constant resistance, widening of a gate electrode (i.e. lengthening of a channel) will bring about not only lowering of TFT operation speed but also large area of TFT part, which will cause an aperture ratio to be lowered in case TFT is used in a liquid crystal display.

BSPR:
Also, in case the etching stopper is thin, there is a possibility that even an **amorphous silicon** region underlying a microcrystal **silicon** region will be in error to be etched, during the etching of the microcrystal **silicon** region, and then a yield will be lowered. Further, in case the microcrystal silicon region is thin, the source/drain region resistance of TFT will be increased and ON/OFF

ratio of TFT will be decreased.

BSPR:
Still more, the etching stopper will remain as it is, at the time of completion
of TFT. The silicon nitride film used for the etching stopper has a nature to
trap electric charge. If electric charge is trapped therein for some reason,
an unwilling channel will be formed in the **amorphous silicon** region 205
thereunder, which will cause a leak of drain current. To avoid this problem,
it is necessary to cause the etching stopper to be two layer structures of
silicon oxide and silicon nitride. In this case, it is needed that the silicon
oxide film be also thick enough, and preferably be 100 nm thick or more.

BSPR:
To overcome the above-mentioned problems, the present invention provides a new
preparing method for TFT using no etching stopper, and also provides TFT
prepared by the method thereof. Further, for purpose of making a microcrystal
silicon region (source/drain) thin, the resistance thereof will be sufficiently
rendered low. Still more, in accordance with the present invention, a sheet of
silicon film will be formed by no way of conventional two-stage processes,
which are the forming of an **amorphous silicon** region (film) to become a channel
forming region, and the forming of a microcrystal **silicon** region (film) to
become a source/drain region. And this one sheet of silicon film will be
reformed partly for a source/drain region and partly for a channel forming
region.

DEPR:
Next, an **amorphous,** semiamorphous, microcrystal, polycrystal,or the
intermediate state thin **silicon** film will be formed, and

patterned with the
mask to form the semiconductor region 105. In many actual cases, an **amorphous silicon** film will be formed considering a film forming temperature and an off
current, but it may be possible that a polycrystal or a semiamorphous **silicon**
is obtained, using such low temperature **crystallization** art as a laser
annealing. In case a polycrystal or a semiamorphous silicon is used, a large
electric field mobility can be obtained, however, it is not suitable for an
active matrix circuit of liquid crystal display panel, because an off-current
increases.

DEPR:
At this situation, firstly an impurity will be selectively implanted into the
semiconductor region 105, by an ion implantation or an ion doping method etc.
thus being formed the impurity region 108. The impurity implantation, however,
brings about very big defects in a semiconductor film, which no longer
functions as a semiconductor. Accordingly, a **crystallization** will be effected
by radiating laser beams from upward. In this laser annealing process, various
conditions of **silicon** ranging from polycrystal but very close to single crystal
to **amorphous** can be formed, by properly controlling a pulse width and an energy
density of the laser beams.

DEPR:
If there is no silicon nitride film 106, the laser beams will reach the region
where functions as a channel forming region not doped with an impurity, and
will enable its part to be **crystallized**. In case where a silicon nitride film
exists, by which a lot of beams will be absorbed, then the **crystallization** will
not occur and the initial situation will be maintained. It is considered .

favorable from the mobility increasing point of view that a channel region will
be **crystallized** by laser beams. The present-day laser technologies, however,
have a deviation in a laser shot-energy, which gives rise to a remarkable
deviation in the **crystallization** degree. As a result, TFT with different
mobilities will be formed.

DEPR:
There is no problem when TFT with a constant mobility is only required. But
the condition will be extremely strict, provided that the mobility is satisfied
with a constant lower limit and further the off-current is satisfied with a
constant upper limit. This comes from the reason that in general TFT with a
big mobility will be also big in the off-current. For example, since not only
the mobility but also the off-current is important factor, in an active matrix
circuit of a liquid crystal display panel, uniformly good TFTs are required.
Accordingly in such case, it is desired that TFT is formed using an **amorphous
silicon** which has a low off-current, even if it has a low mobility, or using a
material which is similar to the **amorphous silicon**. Consequently, in the
present invention, the laser beams should be prohibited from being entered into
a channel forming region by mistake, in the case of such purposes.

DEPR:
This doping process may be done by a laser doping. The **laser** doping is a
method that a sample (a semiconductor film) will be placed in an atmosphere
containing an impurity, and by **irradiating laser** beams or equivalent strong
beams to the sample (semiconductor film) in the atmosphere, the sample surface
will be heated and activated and an impurity gas will be decomposed to diffuse

the impurity over the sample surface. By the laser doping, the impurity is
introduced into the semiconductor film and the semiconductor film is
crystallized. As the impurity gas, in general PH.sub.3 (phosphine) will be
used in case where N-type is furnished, and B.sub.2 H.sub.6 (diborane) will be
used in case where P-type is furnished.

DEPR:
After such doping was executed as above, the silicon nitride film 106 and the
photoresist (will be evaporated by laser beams radiation in most cases) 107
will be removed, and then, the **wiring** 110 and the pixel electrode of ITO
(Indium Tin Oxide) 111 will be formed using the mask 4 and the mask 5 by a
known method. In the above processes, there totally used five sheets of mask,
but these can be reduced to four sheets of mask, by freely using a
self-alignment method as usual. Namely, for the formings of gate electrode,
semiconductor region, as well as pixel electrode and **wiring**, 1-, 1-, and
2-sheet of mask are respectively necessary. The patterning for the silicon
nitride film 106 etc. will be effected by the back exposure (e.g. by
irradiating a light from under the substrate to the mask material (the silicon
nitride film) provided on the semiconductor region), using the gate electrode
as a mask.

DEPR:
In accordance with the present invention, a practical P-channel TFT
(hereinafter referred to as PTFT), which could not be prepared by a
conventional technology in addition to N-channel TFT (hereinafter referred to
as NTFT) prepared mainly with a usual **amorphous silicon TFT**, has come to be
prepared. That is, PTFT has not been practical so far,

because not only the
hole mobility in an **amorphous silicon** of a channel region was small compared
with the ion mobility, but also P-type **silicon** with low enough resistance of
source/drain could not be obtained. In accordance with the present invention,
however, the resistance of P-type silicon has been able to be as low as that of
N-type silicon, and then, PTFT having a practical function of the device has
been able to be prepared.

DEPR:
Therefore, it has begun to be able to prepare a complementary type MOS circuit
(hereinafter referred to as CMOS circuit), using the **amorphous silicon TFT or**
TFT prepared at low temperatures. Up to the present time, the CMOS circuit has
been limited to the high temperature prepared TFT formed on a quartz substrate
at 1000.degree. C. or higher, or the middle temperature prepared TFT formed on
a non-alkali glass substrate at around 600.degree. C. It has been so far
considered that CMOS circuit can not be obtained, using TFT prepared at around
350.degree. C. of the maximum process temperature.

DEPR:
The better **crystallized** state of a semiconductor is, the bigger mobility of
PTFT will be obtained. It is not preferable that the mobility between NTFT and
PTFT is so different from each other, in order to function as CMOS. Though
PTFT with a big mobility can be gotten by enabling a film forming temperature
to be higher, it can not be excessively raised under such condition as
substrate restrictions. But in case where a film is formed at around
350.degree. C. of a substrate temperature using such polysilane as disilane or
trisilane, PTFT, which is seemingly amorphous but its mobility is about one

over several of that of NTFT, will be gotten. Also, it is possible that an
annealing will be carried out in an atmosphere of hydrogen at 300 to
350.degree. C. for 24 hr. or more, after the film forming by CVD plasma
method.

DEPR:
After that, the photoresist mask 309 will be formed in the region of PTFT using
the fourth mask, and laser beams will be radiated in an atmosphere of phosphine
PH.sub.3 as illustrated in FIG. 3(B). Thereby the impurity region 310 of NTFT
(left side) will be formed. Further, the photoresist mask 311 will be formed
in NTFT region using the fifth mask, and laser beams will be radiated in an
atmosphere of diborane B.sub.2 H.sub.6 as illustrated in FIG. 3(C), to form an
impurity region 312 of PTFT (right side). In each laser doping process, laser
beams will be absorbed into the silicon nitride mask, and then the channel
forming regions 313 and 314 will not be **crystallized**.

DEPR:
Then, as shown in FIG. 3(C), the metal wirings (aluminum etc.) 315, 316, 317
will be formed by a known metal **wiring** technology, thus being formed CMOS
circuit consisting of NTFT 318 and PTFT 319. In the above processes, six
sheets of mask are used, but one sheet of mask will be reduced, if the back
exposure technology is used in case of the preparation of silicon nitride masks
307, 308. The doping process will be also conducted by a known ion
implantation or ion doping method. In case where an impurity region is formed
by an ion implantation or an ion doping method, which is capable of a delicate
controlling of an impurity concentration, it is possible to firstly form an
impurity region of either conductivity type in all of TFT,

and then to form an
inverse conductivity type only in a specific TFT, not separately forming both
impurity regions of NTFT and PTFT. In this case, one sheet of mask will be
further reduced. This method, however, can not be applicable to the laser
doping, on account of its difficulty in an impurity controlling.

DEPR:
In the present invention, especially regarding the laser doping, such method as
is shown in FIG. 4 can be also used. This method conducts the doping in a
self-alignment, using the gate electrode as a mask and radiating laser beams
from the back. First of all, in the same way as in the case of FIG. 1, the
gate electrode 402 will be formed using the mask 1 on the substrate 401 which
passes laser beams. If necessary, its oxide 403 will be formed, and also the
gate insulating film 404 will be formed. Then, the semiconductor region 405
will be patterned using the mask 2 (FIGS. 4(A),(B)). Next, laser beams will be
radiated from the back of substrate. This time, the laser beams pass in
parallel in the substrate as illustrated in FIG. 4(C), but are refracted in the
gate electrode where is uneven, and diffracted in the gate electrode etc. thus
resulting in that the parallel passing is injured. Additionally, in such
uneven parts, laser beams are more absorbed in the parts (the oxide layer 403
or the gate insulating film 404), where the laser beams pass through, compared
with the other parts. As a result, the intensity of laser beams will be
extremely lowered on the protrusion part over the gate electrode part, not only
by being masked with a gate electrode but also by the above stated complicated
phenomena. Then, the laser doping will no longer be carried out, and the

initial situation will be kept to become the channel forming region 406. On the other hand, in the other parts, the laser doping will be performed and the impurity region 407 will be formed. Then, it will do well that the metal **wiring** 409 and the pixel electrode 410 etc. is formed using the masks 3 and 4.

DEPR:
Next, the resist was removed (process 6), and the silicon nitride film (104 in FIG. 1) as a gate insulating film was formed, in thickness of 200 nm by a plasma CVD method (process 7). At this time, the substrate temperature was set at 300. After washing of the substrate (process 8), an **amorphous silicon** film was formed in thickness of 30 nm by a plasma CVD method (process 9). The substrate temperature at this time was controlled at 300

DEPR:
Then, a patterning in a semiconductor region was carried out using the mask 2 (process 10), and the **amorphous silicon** film was etched by a reactive ion etching method using CF.sub.4 as a reactive gas (process 11), to form the semiconductor region (105 in FIG. 1). The remaining resist was removed (process 12), and the substrate was washed (process 13).

DEPR:
Next, by an ion doping method, 1.times.10.sup.14 cm.sup.-2 dose of phosphorus ion was implanted (introduced) into the semiconductor region with the silicon nitride mask pattern as a mask using 10 KeV of accelerated energy (process 17), to form the impurity region (108 in FIG. 1). Then, the substrate was washed (process 18), to remove the remaining resist (process 19). And then, a **laser** annealing was executed by **irradiating** XeCl excimer **laser** beam to the semiconductor region with the silicon nitride mask pattern

as a mask (process
20) to **crystallize** the semiconductor region, and the silicon nitride mask
pattern (106 in FIG. 1) was etched with a buffer hydrofluoric acid and removed
(process 21). After that, the substrate was washed
(process 22).

DEPR:
Then, an aluminum film was formed in thickness of 400 nm by a sputtering method
(process 23). The aluminum **wiring** was patterned with the mask 4 (process 24),
and further the aluminum film was etched by a mixed acid (process 25) to form
the aluminum **wiring** (110 in FIG. 1). The remaining resist was removed (process
26). NTFT was prepared through the above processes.

DEPR:
After that, the resist was removed (process 6), and as a gate insulating film,
the silicon nitride film (104 in FIG. 1) was formed in 200 nm thick over the
anodic oxidation film by a plasma CVD method (process 7). At this time, the
substrate temperature was set at 300. After washing of the substrate (process
8), 30 nm thick **amorphous silicon** film was formed by a plasma CVD method
controlling the substrate temperature at 300 (process 9).

DEPR:
Then, the semiconductor region was patterned using the mask 2 (process 10), and
the **amorphous silicon** film was etched by a reactive ion etching method using
CF.sub.4 as a reaction gas (process 11), thereby forming the semiconductor
region (105 in FIG. 1). The remaining resist was removed (process 12), and the
substrate was washed (process 13).

DEPR:
Finally, an aluminum film was formed in thickness of 400 nm by a sputtering
method (process 23), an aluminum **wiring** was patterned using

the mask 4 (process
24), and further an aluminum film was etched with a mixed acid (process 25),
thereby forming the aluminum **wiring** (110 in FIG. 1). The remaining resist was
removed (process 26). Thus, NTFT was prepared by way of the above processes.

DEPR:
Afterward, the resist was removed (process 6), and the silicon nitride film
(404 in FIG. 4) as a gate insulating film was formed in thickness of 200 nm by
a plasma CVD method (process 7). At this time, the substrate temperature was
set at 300. After washing of the substrate (process 8), 30 nm thick **amorphous**
silicon film was formed by a plasma CVD method (process 9). The substrate
temperature at this time was set at 300.

DEPR:
Then, the semiconductor region was patterned with the mask 2 (process 10), and
the **amorphous silicon** film was etched, by a reactive ion etching method using
CF.sub.4 of a reaction gas (process 11), to form the semiconductor region (405
in FIG. 4). The remaining resist was removed (process 12), and the substrate
was washed (process 13).

DEPR:
Next, the **laser** doping of the semiconductor region was performed in a
self-alignment method, using the gate electrode as a mask, and **irradiating** XeCl
excimer **laser** beams to the semiconductor region from the back of the substrate
(from under the substrate) with the semiconductor film being placed in an
atmosphere comprising the impurity (phosphine) (process 14). Since the XeCl
excimer laser was 308 nm in a wave length, it was able to pass through Corning
7059. The substrate temperature during the laser doping was set at 300, and

then the substrate was washed (process 15). The impurity is introduced into the semiconductor film and the semiconductor film is **crystallized** by the laser doping.

DEPR:
After that, an aluminum film was formed in a thickness of 400 nm by a sputtering method (process 16), the aluminum **wiring** was patterned with the mask 4 (process 17). Further the aluminum film was etched with a mixed acid (process 18), and the aluminum **wiring** (409 in FIG. 4) was formed. The remaining resist was removed (process 19). Thus, NTFT was prepared by the above processes.

DEPR:
Then, the resist was removed (process 6), and the silicon nitride film (304 in FIG. 3) as a gate insulating film was formed, in 200 nm thick by a plasma CVD method (process 7). At this time, the substrate temperature was controlled at 300. After washing of the substrate (process 8), 30 nm thick **amorphous silicon** film was formed by a plasma CVD method (process 9). At this time, the substrate temperature was set at 250.

DEPR:
Next, the semiconductor region was patterned with the mask 2 (process 10), the **amorphous silicon** film was etched by a reactive ion etching method using CF.sub.4 of a reaction gas (process 11), and the semiconductor regions (305 and 306 in FIG. 3) were formed. The remaining resist was removed (process 12), and the substrate was washed (process 13).

DEPR:
In the same way, a pattern of PTFT was formed using the mask 5 (process 23), when NTFT was covered with the resist (311 in FIG. 3).

Under this condition,
the doping of boron was executed by a laser doping method in an atmosphere of
diborane (process 24). The impurity (boron) is introduced into a portion of
the semiconductor region 106 which is not covered with the silicon nitride mask
308, and said portion is **crystallized** by the laser beam of the laser doping.
Thus, the P-type impurity region (312 in FIG. 3) was formed. After the laser
doping, the remaining resist (311 in FIG. 3) was removed (process 25), and the
substrate was washed (process 26). Further, the silicon nitride masks (307 and
308 in FIG. 3) were etched with a buffer hydrofluoric acid and removed (process
27). Then, the substrate was washed (process 28).

DEPR:
Finally, an aluminum film was formed in a thickness of 400 nm by a sputtering
method (process 29), an aluminum **wiring** was patterned with the mask 6 (process
30), further, the aluminum film was etched with a mixed acid (process 31), and
the aluminum wirings (315, 316, and 317 in FIG. 3) were formed. The remaining
resist was removed (process 32). NTFT was prepared by the above-mentioned
processes.

CLPR:
13. A method according to claim 10 wherein said impurity doped regions are
crystallized by said light.

CLPR:
17. A method according to claim 14 wherein said impurity doped regions are
crystallized by said light.

CLPV:
irradiating said impurity regions with light from an upper portion of the
insulating film for **crystallizing** the impurity regions wherein said impurity

regions are exposed during said ion doping and said irradiation of light,

CLPV:
forming a semiconductor film comprising **amorphous silicon** over said gate
electrode with the gate insulating film interposed therebetween;

CLPV:
wherein said portion of the semiconductor film is prevented from being
crystallized during the irradiation of said light by said insulating film.

CLPV:
irradiating said impurity regions with a light from an upper portion of the
mask for **crystallizing** the impurity regions wherein said impurity regions are
exposed during said ion doping and said irradiation of light,

CLPV:
forming a semiconductor film comprising **amorphous silicon** over said gate
electrode with the gate insulating film interposed therebetween;

DOCUMENT-IDENTIFIER: US 6124155 A
TITLE: Electro-optical device and thin film transistor and method for forming
the same

---------- KWIC ---------

ABPL:
A method of fabricating silicon TFTs (thin-film transistors) is disclosed. The
method comprises a **crystallization** step by laser irradiation effected after the
completion of the device structure. First, **amorphous silicon** TFTs are
fabricated. In each of the TFTs, the channel formation region, the source and
drain regions are exposed to laser radiation illuminated from above or below
the substrate. Then, the laser radiation is illuminated to **crystallize** and
activate the channel formation region, and source and drain regions. After the
completion of the device structure, various electrical characteristics of the
TFTs are controlled. Also, the amorphous TFTs can be changed into polysilicon
TFTs.

BSPR:
One method of obtaining a polycrystalline, or micro-crystalline, **silicon** film
is to irradiate a completed **amorphous silicon** film with laser radiation, for
crystallizing the amorphous silicon. This method is generally well known.
Laser-crystallized thin-film transistors fabricated by making use of this
technique are superior to **amorphous silicon** thin-film transistors in electrical
characteristics including field effect mobility and, therefore, these
laser-crystallized thin-film transistors are used in peripheral
circuit-activating circuits for active liquid-crystal

displays, image sensors,
and so forth.

BSPR:
The typical method of fabricating a laser-crystallized thin-film transistor is
initiated by preparing an **amorphous silicon** film as a starting film. This
starting film is irradiated with laser radiation to **crystallize** it.
Subsequently, the film undergoes a series of manufacturing steps to process the
device structure. The most striking feature of the conventional manufacturing
process is to carry out the **crystallization** step as the initial or an
intermediate step of the series of manufacturing steps described above.

BSPR:
In accordance with the present invention, in order to make it possible to
crystallize a channel formation region and to activate the Ohmic contact region
of the source and drain by laser irradiation after the device structure of a
thin film transistor is completed, a part of the channel formation region and
parts of the source and drain on the side of the channel formation region are
exposed to incident laser radiation. Alternatively, the source and drain
regions are located on the upstream side of the source and drain electrodes as
viewed from the incident laser radiation, and parts of the source and drain
regions are in contact with the surface of the channel formation region on
which the laser radiation impinges.

BSPR:
characteristics, thus activating the dopant where a group III or V dopant atom
is implanted into an intrinsic **amorphous silicon** film by various methods. In
this way, the electrical conductivity of the film is improved.

BSPV:
(1) Since the laser **crystallization** operation is performed as one step of the
manufacturing process, the electrical characteristics of the thin-film
transistor (TFT) cannot be evaluated until the device is completed. Also, it
is difficult to control the characteristics.

BSPV:
(2) Since the laser **crystallization** operation is effected at the beginning of,
or during, the fabrication of the TFT, it is impossible to modify various
electrical characteristics after the device structure is completed. Hence, the
production yield of the whole circuit system is low.

DEPR:
A TFT (thin film transistor) according to the present invention is shown in
FIGS. 1, (a)-(d). A doped **amorphous silicon** layer to become source and drain
regions and an intrinsic **amorphous silicon** layer to become a channel formation
region can be irradiated with a laser radiation after completion of the device
structure as shown in FIGS. 1(a)-(d) to effectively perform **crystallization** and
activation thereof. In FIG. 1(a), the distance between a source electrode 9
and a drain electrode 10 on a TFT island is set larger than the distance
between a source region 11 and a drain region 12. This permits activation and
crystallization of the source region 11, the drain region 12, and the channel
formation region 5 by laser irradiation from above the substrate.

DEPR:
At this time, laser radiation having a sufficient energy is irradiated to
crystallize even those portions of the intrinsic **amorphous silicon** layer 5
which are under the source and drain regions, the **amorphous**

layer 5 becoming
the channel formation region. In this manner, a channel exhibiting good
characteristics can be obtained. Because the interface between a
gate-insulating film 4 and the channel formation region is below the channel
formation region, the incidence of the laser radiation does not deteriorate the
interface characteristics. Hence, the characteristics of the device are not
impaired.

DEPR:
This can also prevent disturbance of the upper surface of the **amorphous silicon**
film due to the laser irradiation. In particular, if the passivation film is
made of **silicon** oxide, then this passivation film plays the same role as a cap
layer which is generally used at time of **crystallization of an amorphous**
silicon film by laser irradiation. This cap layer is formed on the **amorphous**
silicon film irradiated with laser radiation and prevents disturbance of the
upper surface of the film when it is irradiated with the laser radiation.
Consequently, a laser-crystallized film of high quality can be obtained.

DEPR:
The wavelength of the laser radiation or the material of the glass substrate 1
is so selected that the laser radiation can penetrate through the glass
substrate 1. A base film 2 is formed on the glass substrate to prevent
intrusion of impurities from the substrate. If the material of the base film 2
and the material, e.g., silicon oxide, of the gate insulating film pass the
laser radiation, then the gate electrode 3 is made narrower than the distance
between the source and drain electrodes to permit irradiation of the laser
radiation from below the substrate. As a result, the doped

regions under the source and drain electrodes can be **crystallized** and activated. This further improves various characteristics. If the base layer and the gate insulating film are made of silicon oxide, then they act as cap layers and prevent disturbance of the lower surface of the film.

DEPR:
In FIG. 1(b), the source region 11 and the drain region 12 which are doped are located on the source electrode 9 and the drain electrode 10, respectively, and are in contact with the upper surface of an intrinsic semiconductor layer to become a channel formation region 5. Laser irradiation to the source and drain regions only from above them suffices. Therefore, as compared with the structure shown in FIG. 1(a), various characteristics can be improved more greatly and controlled over wider ranges. In the same way as in the structure of FIG. 1(a), irradiation of laser radiation having a sufficient energy **crystallizes** the portions of an intrinsic **amorphous silicon** layer 5 which are below the source and drain regions, the **silicon** layer 5 becoming a channel formation region. In consequence, a channel having good characteristics can be derived. Since the interface between the gate insulating film 4 and the channel formation region is below the channel formation region, the incidence of the laser radiation does not deteriorate the interface characteristics. Consequently, the characteristics of the device are not deteriorated. If the passivation film consists of silicon oxide, then it serves as a cap layer on irradiation of the laser radiation. The cap layer prevents disturbance of the upper surfaces of the doped **amorphous silicon** film and of the intrinsic **amorphous silicon** film due to the laser irradiation. The

doped **amorphous silicon** film forms the source and drain regions. The intrinsic **amorphous silicon** film is the channel formation region.

DEPR:
Structures shown in FIGS. 1, (c) and (d), are totally inverted versions of the structures of FIGS. 1, (a) and (b), respectively. The wavelength of the laser radiation or the material of the glass substrate is so selected that the laser radiation can penetrate the glass substrate. The laser radiation is irradiated mainly from below the substrate to **crystallize** and activate the source and drain regions as well as the channel formation region.

DEPR:
The structure of FIG. 1(c) is the totally inverted version of the structure of FIG. 1(a). The distance between the source electrode 9 and the drain electrode 10 is set larger than the distance between the source region 11 and the drain region 12, in the same way as in the structure of FIG. 1(a). Laser radiation is illuminated from below the substrate to activate and **crystallize** the source and drain regions and the channel formation region 5.

DEPR:
At this time, laser radiation having a sufficient energy is illuminated to **crystallize** even those portions of the intrinsic **amorphous silicon** layer 5 which are over the source and drain regions, the **amorphous silicon** layer 5 becoming a channel formation region. Thus, a channel having good characteristics can be obtained. Since the interface between the gate insulating film and the channel formation region is located above the channel formation region, the interface characteristics are not deteriorated by the incidence of the laser radiation from below the substrate.

In consequence, the characteristics of the device are not deteriorated.

DEPR:
If the base film 2 that is formed on the glass substrate 1 to prevent intrusion of impurities from the glass substrate is made of **silicon** oxide, then this film acts as a cap layer and prevents disturbance of the lower surfaces of the **amorphous silicon** films some of which are source and drain regions, the remaining **amorphous silicon** film being a channel formation film. If the materials of the passivation film 13 and of the gate insulating film 4 pass the laser radiation such as silicon oxide, then the gate electrode 3 is made narrower than the distance between the source and drain electrodes. Thus, the laser radiation is irradiated from above the substrate to **crystallize** and activate the doped regions located over the source and drain electrodes. Hence, various characteristics can be improved more greatly. At this time, if the passivation film and the gate insulating film are made of **silicon** oxide, they serve as cap layers and can prevent disturbance of the upper surfaces of the **amorphous silicon** films due to the laser irradiation.

DEPR:
In FIG. 1(d), the source region 11 and the drain region 12 which are doped are located under the source electrode 9 and the drain electrode 10, respectively, and are in contact with the undersides of opposite lateral sides of a channel formation region 5. Laser irradiation to the source and drain regions only from below them suffices. Therefore, as compared with the structure shown in FIG. 1(c), various characteristics can be improved more greatly and controlled over wider ranges. In the same way as in the structure of FIG. 1(c),

irradiation of laser radiation having a sufficient energy **crystallizes** the
portions of an intrinsic **amorphous silicon** layer which are above the source and
drain regions, the **silicon** layer becoming a channel formation region. In
consequence, a channel having good characteristics can be derived.

DEPR:
Since the interface between the gate insulating film 4 and the channel
formation region is above the channel formation region, the incidence of the
laser radiation does not deteriorate the interface characteristics.
Consequently, the characteristics of the device do not deteriorate. If the
base film consists of silicon oxide, then it serves as a cap layer on
irradiation of the laser radiation. The cap layer prevents disturbance of the
lower surfaces of the doped **amorphous silicon** film and of the intrinsic
amorphous silicon film due to the laser irradiation. The doped **amorphous**
silicon film forms the source and drain regions. The intrinsic **amorphous**
silicon film is the channel formation region.

DEPR:
In the structure described above, the source and drain regions and the channel
formation region can be activated and **crystallized** by laser irradiation after
the device structure of the **amorphous silicon** thin film transistor has been
completed.

DEPR:
As described thus far, laser radiation is not irradiated before or during
processing of the device structure. Rather, the device is processed during the
fabrication of the **amorphous silicon** TFTs. The laser radiation is directed to
the source, drain regions and to the channel formation

region of desired one or
more of the **amorphous silicon** TFTs after the device
structure is completed
(i.e., the doped semiconductor layers, the intrinsic
semiconductor layer to be
a channel located between source and drain regions adjacent
to a gate electrode
with a gate insulating film therebetween, and the gate
insulating film are
formed, the source and drain regions are formed, the source
and drain and gate
electrodes are formed, and the protective film (passivation
film) are formed)
or after a process including formation of conductive
interconnects is
completed. In this way, the channel formation region of
the thin film
transistor is activated, and the source and drain regions
are activated and
crystallized. At this time, if the electrodes and the
conductive interconnects
have been completed, then the laser irradiation can be
continued while
monitoring electrical characteristics of any desired
amorphous silicon TFT on
the substrate on a real-time basis until an optimum value
is reached. It is
also possible to fabricate thin film transistors having
desired characteristics
by measuring the electrical characteristics subsequent to
laser irradiation and
repeating this series of steps.

DEPR:
In this way, plural **amorphous silicon** TFTs are fabricated
by the same
manufacturing method on the same substrate. After the
device structure is
completed, desired one or more of the **amorphous silicon**
TFTs can be made to
have desired electrical characteristics. That is, TFTs
having different
electrical characteristics on the same substrate can be
manufactured by
irradiation of laser radiation after the device structure
is completed.

DEPR:
After plural **amorphous silicon** TFTs are fabricated by the same manufacturing process on the same substrate and the device structure is completed, desired one or more of the TFTs are **crystallized** by laser irradiation. In this manner, poly-silicon TFTs are fabricated. As a result, a system comprising the substrate on which **amorphous silicon** TFTs and polysilicon. TFTs are fabricated can be manufactured without relying on different manufacturing processes.

DEPR:
An integrated LCD (liquid-crystal display) system consisted of **amorphous silicon** TFTs and polysilicon TFTs. As shown in FIG. 2, this integrated LCD system needed TFTs 30 for activating pixels arranged in rows and columns, as well as TFTs 31 for peripheral circuits. These two kinds of TFTs were required to operate at totally different speeds. A mobility of about 1 cm.sup.2 /V.multidot.s suffices for the TFTs for activating the pixels. On the other hand, the TFTs for the peripheral circuits must operate at a high speed on the order of several megahertz. Preferably, therefore, the TFTs for the activation of the pixels are made of **amorphous silicon,** while the TFTs for the peripheral circuits are made of polysilicon. In this example, the **amorphous silicon** TFTs and the polysilicon TFTs could be manufactured simultaneously by the same process for fabricating the device structure of the system shown in FIG. 2.

DEPR:
An intrinsic **amorphous silicon** film 5 was formed on the gate-insulating film 4 by PCVD. The thickness of the film 5 was 200 to 1000 .ANG.. In the present example, the thickness was 700 .ANG.. Silane (SiH.sub.4) was used as the raw

material gas. The film was formed at a temperature of 150 to 300.degree. C.
In the present example, the temperature was 200.degree. C.

DEPR:
A doped **amorphous silicon** layer 6 was formed on the intrinsic **amorphous silicon**
film 5 by FCVD. In the present example, the layer 6 was an n.sup.+ -type
amorphous silicon layer. The thickness of the layer 6 was 300 to 500 .ANG..
In the present example, the thickness was 500 .ANG..
Silane was used as the
raw material gas. Phosphine (PH.sub.3) which accounted for 1% of the silane
was added to implant phosphorus as an n-type dopant. The film was formed at a
temperature of 150 to 300.degree. C. In the present example, the temperature
was 200.degree. C. The RF frequency was 13.56 MHz. The RF output power was 40
W. The pressure was 0.5 torr. The deposition rate was 60 .ANG./min.

DEPR:
The gate insulating film 4, the intrinsic **amorphous silicon** layer 5, and the
n.sup.+ -type **amorphous silicon** layer 6 were formed in this way, thus resulting
in a laminate shown in FIG. 3(C). These layers were all created by PCVD.
Therefore, it is effective to form them in succession in a multi-chamber
system. Other methods such as low-pressure CVD, sputtering, photo-assisted CVD
may also be adopted. Subsequently, a dry etching process was performed, using
a second photomask P2, to form a TFT island as shown in FIG. 3(D).

DEPR:
Then, a chromium layer 7 which would become source and drain electrodes was
formed by sputtering. The resulting laminate is shown in FIG. 3(E). The
thickness was 500 to 1000 .ANG.. In the present example, the thickness was 800

.ANG.. This layer was patterned, using a third photomask P3. At this time,
the n.sup.+ -type **amorphous silicon** layer was patterned by dry etching without
peeling off resist 8. Thus, a channel formation region, a source electrode 9,
a drain electrode 10, a source region 11, and a drain region 12 were formed,
resulting in a laminate shown in FIG. 3(F).

DEPR:
A wet etching process was carried out without peeling off the resist to perform
an overetching process which made the distance between the source and drain
electrodes larger than the distance between the source and drain regions. This
made it possible to activate and **crystallize** the source and drain regions by
laser irradiation from above the laminate. Thereafter, the resist was peeled
off, producing a laminate shown in FIG. 3(G).

DEPR:
In this way, either the channel formation region or the source and drain
regions or all of them were illuminated with laser radiation while monitoring
the electrical characteristics on the measuring instrument. As a result, the
region or regions were **crystallized** and activated. TFTs for activating the
matrix of pixels 30 shown in FIG. 2 exhibited desired characteristics. These
TFTs are huge in number, e.g., 640.times.400=256,000. It is necessary that
these TFTs have exactly the same characteristics. Hence, it has been very
difficult to increase the production yield. The novel method could greatly
reduce defective TFTs whose characteristics deviate greatly from intended
characteristics. Consequently, the production yield could be enhanced greatly.

DEPR:
TFTs 31 (FIG. 2) for peripheral circuits were sufficiently

illuminated with
laser radiation. The result is that the characteristics were improved greatly.
Before the laser illumination, the field effect mobility .mu..sub.1 was 0.5 to
0.8 cm.sup.2 /V.multidot.s and the threshold voltage V.sub.th1 was 10 to 20 V.
After the laser illumination, the field effect mobility .mu..sub.2 was 10 to
100 cm.sup.2 /V.multidot.s and the threshold voltage V.sub.th2 was 5 to 7 V. In
this way, the characteristics were improved greatly. The TFTs could operate at
a sufficiently large velocity to activate the peripheral circuits of a liquid
crystal display device. The channel formation region made of an **amorphous**
silicon film was **crystallized** and became a polysilicon film having a high
carrier mobility. The TFTs had satisfactory characteristics as polysilicon
TFTs.

DEPR:
As described thus far, in order to **crystallize** and activate the channel
formation region, the source and drain regions by laser irradiation after the
completion of the device structure, it is necessary that the incident side, or
the passivation film at the top of the laminate, pass ultraviolet radiation.
In the channel formation region, it is the interface with the gate insulating
film which operates as a channel in practice. Therefore, the intrinsic
amorphous silicon layer which becomes the channel formation region must be
crystallized sufficiently. For this purpose, this **amorphous silicon** layer
should be made as thin as possible.

DEPR:
In this way, the various characteristics can be controlled and polysilicon TFTs
can be fabricated by **irradiating the amorphous silicon** TFTs with **laser**

radiation after the device structure is completed. Also, the **amorphous silicon** TFTs and the polysilicon TFTs can be manufactured separately on the same substrate during the same process for fabricating the same device structure.
Furthermore, a circuit system having numerous polysilicon TFTs can be fabricated at a low temperature between room temperature and 400.degree. C.
The system can be manufactured economically without using an expensive glass such as quartz glass.

DEPR:
A polysilicon TFT liquid-crystal display having redundant circuit configurations was fabricated in accordance with the present invention. It is very difficult to completely operate all TFTs of a circuit system using numerous polysilicon TFTs such as a polysilicon TFT liquid-crystal display. In reality, some form of redundant configuration is often adopted to improve the production yield. One kind of redundant configuration for **amorphous silicon** TFTs for activating the matrix of pixels of an **amorphous silicon TFT** liquid-crystal display comprises two TFTs connected in parallel. These two TFTs are operated simultaneously. If one of them does not operate for some cause or other, the other operates. This improves the production yield.
However, the electric current flowing through one polysilicon TFT when it is conducting is as large as about 0.1 mA, which is approximately 100 times as high as the current of about 1 .mu.A flowing through a conducting **amorphous silicon TFT**. If twice as many as TFTs are operated for redundancy, then it follows that an exorbitant amount of current is wasted. Therefore, it is desired that each one pixel be activated by one TFT.

DEPR:
FIG. 5 shows the arrangement of the TFTs for activating pixels 29 arranged in rows and columns. These TFTs were **amorphous silicon** TFTs. Two TFTs were connected in parallel. Each pair of TFTs were connected with every pixel electrode 30. One of these two TFTs, TFT 23 in this example, was irradiated with laser radiation to make the TFT a polysilicon TFT. A measuring instrument was connected, and the operation was checked. If no trouble was found, then the operator went to the next step. Since the redundant TFT 24 was an **amorphous silicon TFT,** the working current was two orders of magnitude less than the working current through a polysilicon TFT. Therefore, the effects of redundant TFT could be substantially neglected. Furthermore, parallel operation does not occur, because the threshold voltage for a polysilicon TFT was 0 to about 10 V, whereas the threshold voltage for an **amorphous silicon TFT** was about 10 to 20 V. In this manner, only the laser-crystallized polysilicon TFT operated.

DEPR:
If any TFT does not operate normally, the redundant **amorphous silicon TFT** (24 in this example) forming a pair with the malfunctioning TFT is irradiated with laser radiation to make the **amorphous silicon TFT** a polysilicon TFT. If necessary, the interconnect to the non-redundant TFT, or point A in this example, is broken by the laser irradiation. In this manner, the operated TFT can be easily switched to the redundant TFT.

DEPR:
The redundant circuit of the shift register also comprises two same circuits connected in parallel. After the condition shown in FIG. 3(H), the TFTs are

fabricated as **amorphous silicon** TFTs until electrodes are connected. Later connection or switching using a connector or the like may also be made. All the TFTs in one circuit, 21 in this example, are **crystallized** by laser irradiation. A measuring instrument is connected to check the operation. If they operate normally, then the operator goes to the next step.

DEPR:
Where both circuits are connected in parallel, the TFT in the redundant circuit is an **amorphous silicon TFT** and, therefore, the working current is about two orders of magnitude smaller than the working current through a polysilicon TFT. Hence, the effects of the TFT in the redundant circuit are substantially negligible. Furthermore, parallel operation does not occur, because the threshold voltage for a polysilicon TFT is 0 to about 10 V, whereas the threshold voltage for an **amorphous silicon TFT** is about 10 to 20 V. In this manner, only the laser-crystallized polysilicon TFT operates.

DEPR:
If the circuit does not operate normally, the **amorphous silicon TFT** in the redundant circuit 22 is irradiated with laser radiation to change the **amorphous silicon TFT** into a polysilicon TFT. If necessary, the interconnect (point B in this example) to the non-redundant circuit is broken by laser radiation. In this way, the operated circuit is easily switched to the redundant circuit. Of course, the connection or switching may be made by a connector or the like.

DEPR:
Consequently, **crystallization** by laser irradiation is not needed unless the necessity of switching to the redundant circuit arises.

The time for which
laser radiation is irradiated is halved compared with the case in which all
TFTs are irradiated with laser radiation at the beginning of, or during, the
process for manufacturing them. As such, wasteful consumption of energy is
avoided. Also, the process time is shortened. A reduction in the cost is
accomplished. Furthermore, energy is saved. In addition, the operation for
switching the operated TFT to the redundant TFT can be quite easily performed
without involving complex **wiring** operations.

DEPR:
as the mobility of the thin film transistors on the same substrate to be
controlled at will. Also, a mixed system comprising **amorphous silicon** TFTs and
polysilicon TFTs can be fabricated by **crystallizing** only requisite TFTS.

DEPR:
The novel TFT structures and general TFT structures are manufactured on the
same substrate, making use of **amorphous silicon**. Laser radiation is directed
to the TFTs of the novel structure. Thus, a mixed system comprising **amorphous**
silicon TFTs and polysilicon TFTs can be realized.

CLPR:
3. A method according to claim 1 wherein said first semiconductor film
comprises intrinsic **amorphous silicon**.

CLPR:
9. A method according to claim 7 wherein said first semiconductor film
comprises intrinsic **amorphous silicon**.

CLPR:
15. A method according to claim 13 wherein said first semiconductor film
comprises intrinsic **amorphous silicon**.

CLPR:
21. A method according to claim 19 wherein said first semiconductor film
comprises intrinsic **amorphous silicon**.

CLPR:
27. A method according to claim 25 wherein said first semiconductor film
comprises intrinsic **amorphous silicon**.

CLPR:
33. A method according to claim 31 wherein said first semiconductor film
comprises intrinsic **amorphous silicon**.

CLPR:
39. A method according to claim 37 wherein said first semiconductor film
comprises intrinsic **amorphous silicon**.

CLPR:
45. A method according to claim 43 wherein said first semiconductor film
comprises intrinsic **amorphous silicon**.

CLPR:
51. A method according to claim 49 wherein said first semiconductor film
comprises intrinsic **amorphous silicon**.

CLPV:
forming a first semiconductor film comprising **amorphous silicon** over said gate
electrode with said gate insulating film interposed therebetween;

CLPV:
forming a first semiconductor film comprising **amorphous silicon** over said gate
electrode with said gate insulating film interposed therebetween;

CLPV:
forming a first semiconductor film comprising **amorphous silicon** over said gate
electrode with said gate insulating film interposed therebetween;

CLPV:
forming a first semiconductor film comprising **amorphous silicon** over said gate
electrode with said gate insulating film interposed therebetween;

CLPV:
forming a first semiconductor film comprising **amorphous silicon** over said gate
electrode with said insulating film interposed therebetween;

CLPV:
forming a first semiconductor film comprising **amorphous silicon** over said gate
electrode with said gate insulating film interposed therebetween;

CLPV:
forming a first semiconductor film comprising **amorphous silicon** over said gate
electrode with said gate insulating film interposed therebetween;

CLPV:
forming a first semiconductor film comprising **amorphous silicon** over said gate
electrode with said gate insulating film interposed therebetween;

CLPV:
forming a first semiconductor film comprising **amorphous silicon** over said gate
electrode with said gate insulating film interposed therebetween;

ORPL:
C. Hayzelden et al., "In Situ Transmission Electron Microscopy Syudies of
Silicide-Mediated **Crystallization of Amorphous Silicon**",
Appl. Phys. Lett.,
vol. 60, No. 2, (Jan. 13, 1992), pp. 225-227.

ORPL:
A.V. Dvurechenskii et al., "Transport Phenomena in

Amorphous Silicon Doped by
Ion Implantation of 3d Metals", Phys. Stat. Sol., vol. A95,
(1986), pp. 635-640
Month Unknown.

ORPL:
T. Hempel et al., "Needle-Like **Crystallization** of Ni Doped
Amorphous Silicon
Thin Films", Solid State Communications, vol. 85, No. 11,
(Mar. 1993), pp.
921-924.

CLIPPEDIMAGE= JP406089905A
PAT-NO: JP406089905A
DOCUMENT-IDENTIFIER: JP 06089905 A
TITLE: THIN FILM SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUBN-DATE: March 29, 1994

INVENTOR-INFORMATION:
NAME
YAMAZAKI, SHUNPEI
CHIYOU, KOUYUU
TAKEMURA, YASUHIKO

ASSIGNEE-INFORMATION:

NAME	COUNTRY
SEMICONDUCTOR ENERGY LAB CO LTD	N/A

APPL-NO: JP05167502
APPL-DATE: June 14, 1993

INT-CL_(IPC): H01L021/336; H01L029/784

ABSTRACT:
PURPOSE: To improve the crystallinity of a semiconductor film by **irradiating** the semiconductor film with pulsed **laser** light or similar strong light not by a thermally equilibrium process.

CONSTITUTION: After a semiconductor film 103 is formed on an **insulating** substrate 101, a transparent protective film 104 is formed on the film 103.
Then the surface of the film 103 is exposed by removing the film 104, and the exposed part of the film 103 is crystallized by **irradiating** the exposed part with pulsed **laser** light or the light of a halogen **infrared** lamp. After forming a gate **insulating** film 107 on the film 103, metallic **wiring** 122-124 is formed on the film 107 and ions are implanted at a high speed in a self-aligning way by using the **wiring** 122-124 as a mask. After implanting

the ions, the film 107
is irradiated with pulsed laser light or the light of the halogen infrared lamp
by using the **wiring** 122-124 as a mask. Therefore, a **TFT** excellent in
characteristic and reliability can be manufactured at high yield.